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Analysis of Multiphase Bidirectional Non-Isolated DC to DC Converter for High Power Applications

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Abstract

For high-power energy storage systems, this article introduces a new multi-phase interleaved bi-directional dc/dc power converter that can connect two dc sources with differing voltage levels. When the filter voltage and current ripples are four times more than the switching frequency, the converter is suggested to decrease input and output ripples as well as the size of passive components. By dividing the current evenly across the switch branches of the converter and using a multi-phase interleaving approach to lower conduction loss, the linked inductor allows for a better power density. In various power transfer modes, the theoretical analysis and functioning of the converter are shown. Additionally, the findings of the simulation and the fundamental operating principle are detailed. It demonstrates how the converter works in both the incoming and outgoing power directions.

Keyword: Bi-directional dc/dc converter, high-power dc/dc converter, multi phase dc/dc converter, interleaved operation, coupled inductors

Introduction

Hybrid and electric vehicles, as well as other continuous power supply, use or need energy storage, and have many industrial, military, agricultural, and aerospace applications. To ensure safe, stable, and faultless functioning, almost all of these systems use accumulators or other energy buffers because of the space constraints ^[1]. In order to keep the accumulators' effective power transfer capacity to the external system from being reduced, these applications prioritise power density and high efficiency in system integration. Because of their importance in managing energy flows and maintaining bus voltage stability, bidirectional dc/dc converters are essential for connecting energy storage devices to different power systems, including batteries, ultracapacitors, and supercapacitors ^[2].

One example of an ESS is shown in Figure 1, which includes a bidirectional dc/dc converter, a dc/ac inverter, and batteries or ultracapacitors. Applications requiring voltage matching and control of power flow between two systems often make use of dc/dc converters. As an interface to energy storage

devices, however, many bi-directional dc/dc converters have been researched and developed, each with a focus on a distinct use ^[3]. In addition to being utilised for a wide range of power and voltage levels, these buck and boost type converters are also that of as non-isolated. Various non-isolated topologies for power transmission have been proposed in the literature.

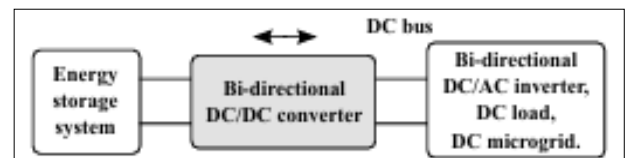


Fig 1: Basic block diagram configuration for the ESS

To facilitate energy storage in ESSs, this article suggests a MIGIC, or multi-phase interleaved bidirectional dc/dc converter with linked inductor, which can connect to dc microgrids, batteries, ultracapacitors, and bidirectional dc/ac inverters. The converter suggested in ^[4] serves as the basis for

the circuit depicted in Figure 2. The efficiency of the converter is enhanced by the suggested design, which offers some benefits over competing designs in areas like current splitting and minimising rms current stress in semiconductors. System reliability is improved in high power applications by reducing input current ripple and using current ripple cancellation for $D = 1/4$ and $1/2$. This is achieved by using the smallest size of passive components. According to [5], the circuit provides a topology with a high power density, improves the efficiency of non-isolated bi-directional dc/dc converters, and makes the system very reliable. The input inductor's high-frequency switching current ripple may be cancelled via interleaved operation with many phases, leading to a decrease in the filter, improved dynamic responsiveness, and increased efficiency. Consequently, the converter may be suitable for use as an ESS's power electronic interface [6].

We provide an idealised theoretical analysis of the suggested converter after studying it in continuous conduction mode (CCM).

Research Objective

An analysis of the operational properties and performance of a high-power energy-storage application-specific multiphase interleaved bidirectional non-isolated DC-DC converter is the primary objective of this work. The topics covered in this study include voltage conversion ratio, current sharing, size of passive components, bidirectional buck-boost operation,

inductor current ripple reduction, and comparison with traditional converter topologies in terms of performance.

Research Gap

Excessive power operation causes traditional non-isolated bidirectional DC-DC converters to suffer from excessive current ripple, semiconductor stress, and large passive components. While interleaved topologies do a better job of sharing current, there is still room for improvement in ripple cancellation and power density. Interleaving and linked inductors in the current multiphase design improve current distribution, ripple, and passive components.

Proposed Bidirectional DC/DC Converter

Presented in Figure 2 is the suggested architecture, which comprises a three-inductance configuration with two of them linked to form a negative-coupled inductor, a four-leg interleaved configuration with eight switches, eight diodes, and two capacitors. The $Q_{1a}...4a$ switches are used for buck operation, whereas the $Q_{1b}...4b$ switches are used for pulse width modulation (PWM) switching in boost operation. When current flows from the low-voltage (LV) side (E_1) to the high-voltage (E_2) side (E_2), the circuit goes into boost mode to drain the LV-side battery or ultracapacitors while maintaining a certain HV-side voltage. The circuit uses buck mode to recharge the battery or ultracapacitors while the power flow is in the opposite direction [7].

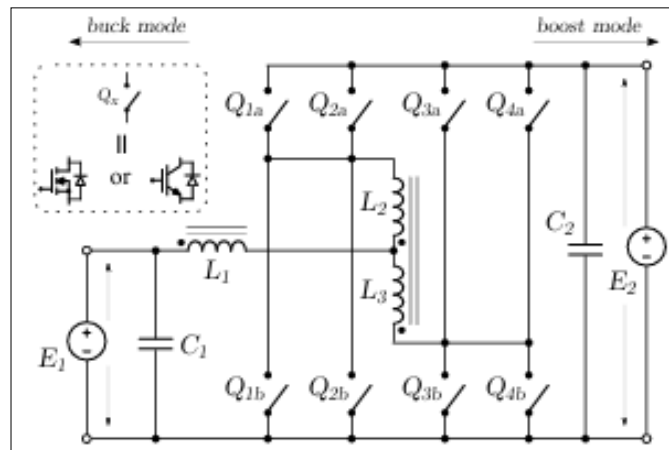


Fig 2: A proposed MIBIC circuit diagram for a coupled inductor-based bidirectional dc/dc converter

As shown in Figure 3, the circuit is divided into two distinct operating areas. The amount of overlapping switches is what differentiates them from one another [8]. The duty cycle ranges from zero to half, and its value could be different for each area.

To achieve a ripple frequency of two on the coupled inductor and four on the input inductor current at the same switching frequency, the sequencing of driving signals is critical [9].

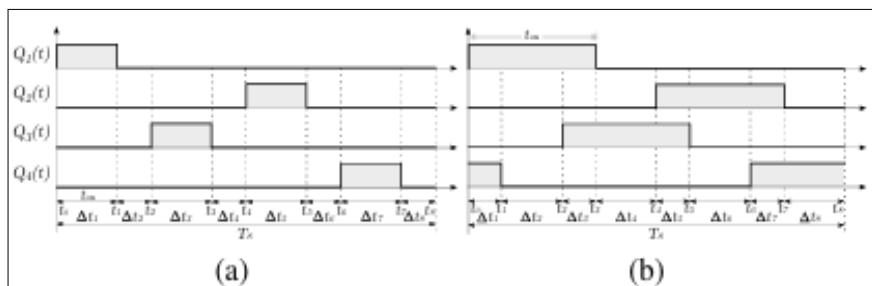


Fig 3: Signals that drive the power switch: (a) A modulation strategy for the range of $0 \leq D \leq 1/4$, and (b) a modulation scheme for the range of $1/4 \leq D < 1/2$

The next sections outline the two power flow directions' operational principles and steady-state analyses.

A. Advantages of Proposed Converter

The suggested architecture has many benefits, the most

important of which are a smaller footprint, better power density, less RMS current stress on semiconductor devices, balanced current sharing across converter phases, and less input-current ripple^[10]. This design is ideal for energy storage systems with a lot of power since the effective ripple frequency is increased by the four-phase interleaved switching arrangement^[11].

Analysis and Basic Operating Principle

Assumptions that demonstrate the topological principle are as follows: 1) the converter is in steady state; 2) all components are ideal (no losses); 3) the switches have a on time ($t_{on}=DT_s$) during steady state operation and the switching period is $T_s=1/f_s$; 4) all switches have the same duty cycle, $\Delta t_1=\Delta t_3=\Delta t_5=\Delta t_7$ and $\Delta t_2=\Delta t_4=\Delta t_6=\Delta t_8$; 5) the coupled inductor has infinite magnetising inductance and unitary coupling factor; 6) the turn ratio of the coupled inductor is unitary ($nL=1:1$); 7) the capacitances are large enough to consider a constant output voltage; 8) the magnetic flux in the inductors is continuous, meaning that the converter is operating in CCM; 9) the switching pattern is shifted by $\pi/2$ ^[12].

A. Operational principle in boost mode

Power is transferred from the direct current source E_1 to the load, which is symbolised by its resistance R_1 , while the system is operating in boost mode.

1. Operation in $D < 1/4$ region, with driving gate signals depicted in Figure 3(a)

As seen in Figure 4(a): Initial Phase (t_0, t_1): While Q_{2b} , Q_{3b} , and Q_{4b} are not active, Q_{1b} is. The forward bias is present in diodes D_{3a} and D_{4a} . Power is fed into the circuit from the source, input inductor current grows linearly, and the load receives energy from the linked inductor's magnetising inductance all at once. Inductor voltage equations are derived from Kirchhoff's voltage law.

$$v_{L1}(t) = E_1 - 2E_2, \Delta t_1 = t_1 - t_0 = DT_s \quad (1)$$

$$v_{L2}(t) = 2E_2, v_{L3}(t) = -2E_2 \quad (2)$$

Phase Two (t_1, t_2), Phase Three (t_3, t_4), Phase Six (t_5, t_6),

and Phase Eight (t_7, t_8); [refer to Figure 4(b)] during these times, all the switches are switched off at t_2, t_4, t_6 , and t_8 . Every one of the four diodes D_{1a} , D_{2a} , D_{3a} , and D_{4a} are biased forward. At the same time as the source supplies energy to the complete circuit, the input inductor current falls linearly and the energy stored in the magnetising inductances continues to flow to the load and output capacitor C_2 .

$$v_{L1}(t) = E_1 - E_2, \Delta t_2 = t_2 - t_1 = 41 - 4DT_s \quad (3)$$

$$v_{L2}(t) = 0, v_{L3}(t) = 0 \quad (4)$$

Level Three [(t_2, t_3) ; refer to Figure 4(c)]: When t_2 rolls around, Q_{3b} turns on, and D_{1a} and D_{2a} start conducting. The linked inductor receives some of the energy from the dc source, while the load receives the remainder. Here are the voltage equations for a connected inductor.

$$v_{L2}(t) = -2E_2, v_{L3}(t) = 2E_2 \quad (5)$$

Stage five, as shown in Figure 4(d), is identical to stage one. At time t_4 , D_{3a} and D_{4a} begin conducting, and Q_{2b} switches on.

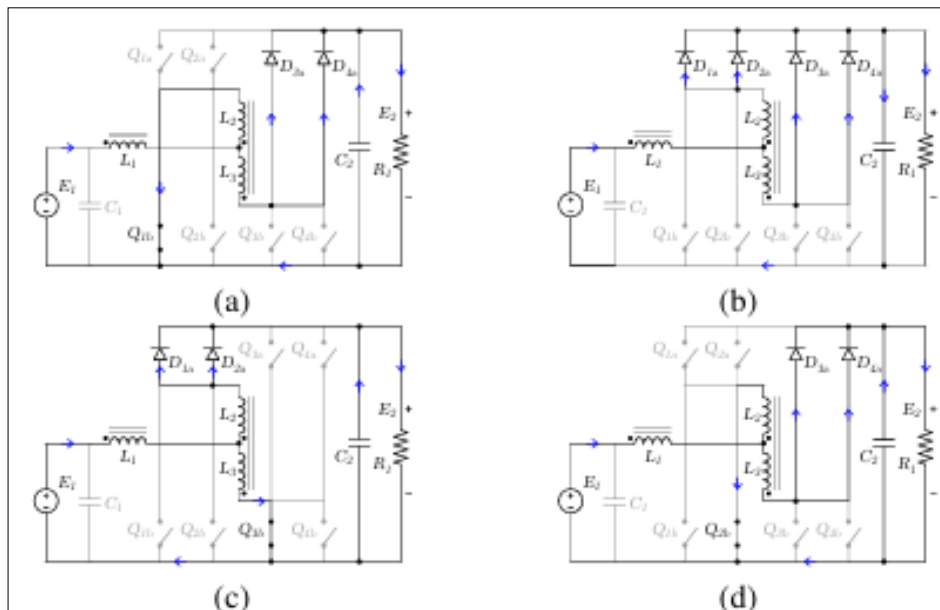
Stage Seven [(t_6, t_7) ; refer to Figure 4(e)]: Very much like the third stage. Conduction from D_{1a} and D_{2a} begins at t_6 , when Q_{4b} becomes active. Reverse bias is seen in diodes D_{3a} and D_{4a} ^[13].

2. Operation in $1/4 \leq D < 1/2$ region, with driving gate signals depicted in Figure 3(b)

Beginning Phase [(t_0, t_1) ; refer to Figure 5(a)]: All of the diodes $D_{1a} \dots D_{4a}$ are inverted, and Q_{1b} and Q_{4b} are turned on. The inductors act as energy storage devices, allowing the power dc source to be transferred to the load by a linear rise in current and discharge of the output capacitor C_2 . Equations (4) provide the voltage equations over the linked inductor, and the input inductor may be represented as:

$$v_{L1}(t) = E_1, \Delta t_1 = 44D - 1T_s \quad (6)$$

This is comparable to the first stage for the $D < 1/4$ area in the second stage (t_1, t_2), as shown in Figure 4(a). When Q_{4b} is turned off at time t_1 , D_{3a} and D_{4a} begin to conduct.



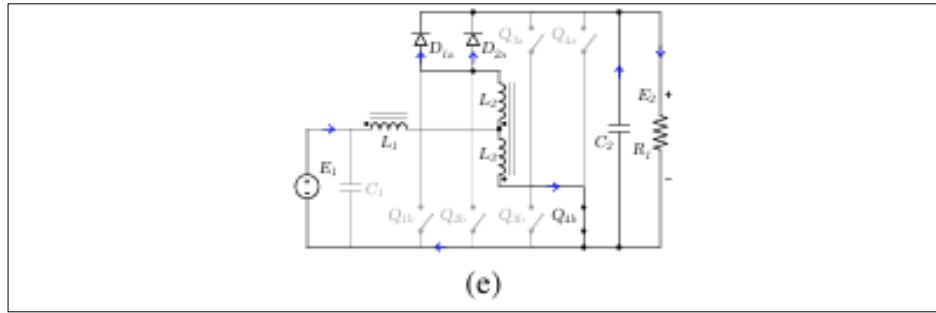


Fig 4: The converter topological stages that have been suggested for boost mode ($D \leq 1/4$) are as follows: (a) condition $[t0, t1]$, (b) conditions $[t1, t2]$, $[t3, t4]$, $[t5, t6]$ and $[t7, t8]$, (c) condition $[t2, t3]$, (d) condition $[t4, t5]$, and (e) condition $[t6, t7]$

Equations (1) and (2) provide the voltage across the inductor, and by

$$\Delta t_2 = 2T_s - 2DT_s \quad (7)$$

At t_2 , Q_{3b} is switched on, and Q_{1b} remains in the turn-on condition throughout the Third Stage $[(t_2, t_3)]$; see Fig. 5(b). The second stage is very much like the first.

The intervals in the fourth stage are distinct from those in the third stage for the $D < 1/4$ region (see Figure 4(c)). With Q_{3b} remaining in the turn-on condition at t_3 , D_{1a} and D_{2a} start conducting, and Q_{1b} is turned off. You may find the connected inductor's voltage formulae in (5).

During this period, Q_{3b} is kept ON, and Q_{2b} is switched ON at time t_4 , in the Fifth Stage $[(t_4, t_5)]$; see Figure 5(c). This pause is analogous to the initial and final phases ^[14].

The sixth stage is comparable to the fifth stage for the $D < 1/4$ area (see Figure 4(d)). At time t_5 , D_{3a} and D_{4a} start conducting, and Q_{3b} is shut off while Q_{2b} is still turned on. Similar to the second stage, the inductors have a voltage.

Stage Seven $[(t_6, t_7)]$; see Figure 5(d): At t_6 , Q_{4b} is switched on, while Q_{2b} is still in the turn-on stage. The first, third, and fifth phases are analogous to this period.

See Figure 4(e) for the Eighth Stage, which is comparable to the Seventh Stage for the $D < 1/4$ area. Since Q_{4b} is still in the on state at t_7 , D_{1a} and D_{2a} begin conducting, and Q_{2b} is switched off. Just as in Stage 4, the voltage across the inductors remains constant.

In order to get the voltage gain for the proposed converter's CC-MO, we need to take the average voltage across inductor L_1 and express it as.

$$\overline{V_L}(t) = \frac{4}{T_s} \left[\int_0^{\Delta t_1} v_{L1}(t) dt + \int_0^{\Delta t_2} v_{L1}(t) dt \right] = 0 \quad (8)$$

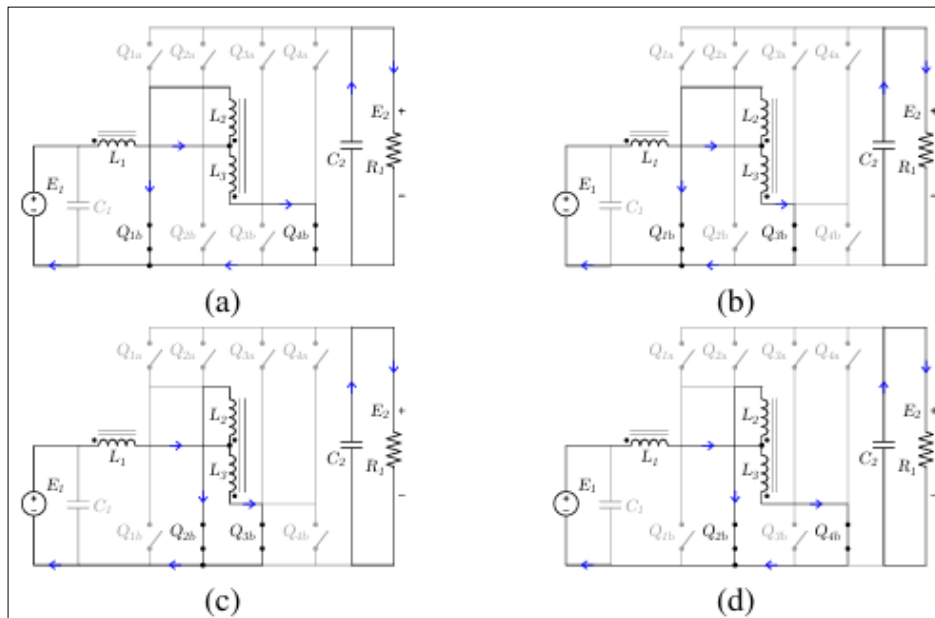


Fig 5: The recommended converter's topological stages in boost mode ($1/4 \leq D < 1/2$) are as follows: (a) state $[t0, t1]$, (b) state $[t2, t3]$, (c) state $[t4, t5]$, and (d) state $[t6, t7]$.

If we replace the inductor voltage (1), (3) or (6), (1) with (8), we may get the voltage gain while the converter is operating in boost mode as

$$M_1 = \frac{E_2}{E_1} = \frac{1}{1 - 2D} \quad (9)$$

The DC voltage gain of the suggested converter in boost operation is graphically compared to that of the traditional Boost converter, which is identical to that of ^[15] (Figure 8(a)). One way to represent the average inductor current value is as:

$$E_1 \cdot I_{L1} = E_2 \cdot I_{R1}; \quad I_{L1} = \frac{E_2}{(1 - 2D) R_1} \quad (10)$$

$$I_{L2} = I_{L3} = \frac{E_2}{2(1-2D)R_1} \quad (11)$$

Operational principle in buck mode

The load, shown by its resistance R_2 , receives power in the buck mode from the dc source E_2 .

1. Operation in $D < 1/4$ region

At time zero, the first stage is shown in Figure 6(a): Q_{1a} is turned on while $Q_{2a}...4a$ are turned off. Forward biased diodes are D_3 and D_4 . The energy in the linked inductor's magnetising inductance is transferred to the load and output capacitor C_1 simultaneously as the source supplies power to the circuit, causing the current thru the output inductor to rise linearly. A representation of the output inductor is provided by (2), which also gives the voltage equations across the connected inductor:

$$v_{L1}(t) = \frac{E_2}{2} - E_1 \quad (12)$$

During the second, fourth, sixth, and eighth stages, as shown in Figure 6(b), the switches are turned off at times t_2 , t_4 , t_6 , and t_8 , respectively. Every one of the diodes $D_{1b}...4$ have a forward bias. In equation (4), we get the voltage across the linked inductor.

$$v_{L1}(t) = -E_1 \quad (13)$$

Step Three: At time t_2 , the Q_{3a} is turned on and the D_{1b} and D_{2b} begin conducting (refer to Figure 6(c)). In (5) we get the linked inductor's voltage equations, and in (12) we find those for the output inductor.

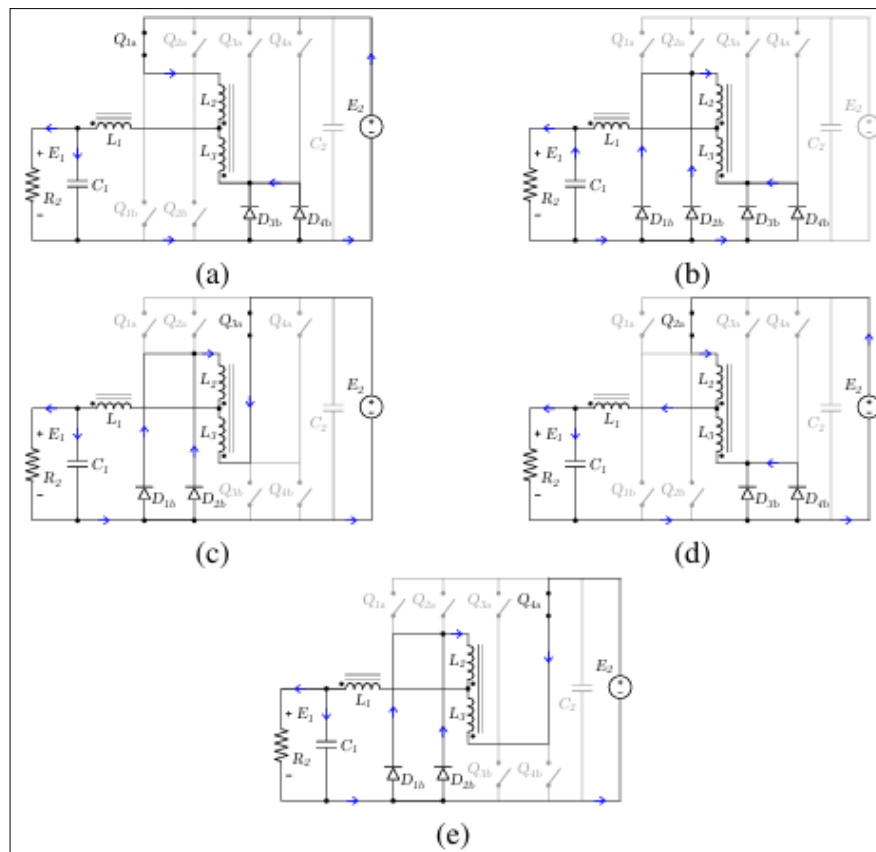


Fig 6: In the topological phases of the converter that has been suggested for buck mode, where D is less than or equal to one fourth, there are the following states: (a) $[t_0, t_1]$, (b) $[t_1, t_2]$, $[t_3, t_4]$, $[t_5, t_6]$ and $[t_7, t_8]$, (c) $[t_2, t_3]$, (d) $[t_4, t_5]$, and (e) $[t_6, t_7]$

See Figure 6(d) for the fifth step, which is the same as the first stage (t_4, t_5). The Q_{2a} is switched on at t_4 , and D_{3b} and D_{4b} start conducting at that time [16].

The seventh stage is identical to the third stage (t_6, t_7 ; see Figure 6(e)). When t_6 rolls around, the Q_{4a} turns on and D_{1b} and D_{2b} begin to conduct. You may reverse-bias diodes D_{3b} and D_{4b} . 2) during the $1/4 \leq D$ First Stage (t_0, t_1), as shown in Figure 7(a), all diodes $D_{1b}...4b$ are inverted, and Q_{1a} and Q_{4a} are turned on. A linear rise in the inductor current stores the dc power source's energy, and capacitor C_1 charges as an output. Equations (4) describe the connected inductor's voltage, while the following describes the output inductor:

$$v_{L1}(t) = E_2 - E_1 \quad (14)$$

Second Stage $[(t_1, t_2)]$; see Figure 6(a)]. This is similar to first stage for $D < 1/4$ region. At t_1 , the Q_{4a} is OFF but Q_{1a} is still in the turn on state. The voltage equations across the inductors are expressed in (12) and (2). Third Stage $[(t_2, t_3)]$; see Figure 7(b)]: Q_{1a} is still in the turn on state and at t_2 the Q_{3a} is turned on. This period is similar to the first phase. Fourth Stage $[(t_3, t_4)]$; see Figure 6(c)]: This region is similar to the third stage for $D < 1/4$ region. At t_3 , the Q_{1a} is turned OFF and the Q_{3a} is still in the turn-on state. The voltage equations of the coupled inductor are given by (5) [17]. Fifth Stage $[(t_4, t_5)]$; see Figure 7(c)]: During this interval, Q_3 is still in turn on state and at t_4 the Q_2 is turned on. This interval is similar to the first and third stages. Sixth Stage $[(t_5, t_6)]$; see Figure 6(d)]: Similar to the fifth stage for the region $D < 1/4$. At t_5 , the Q_{3a} is turned OFF but Q_2 is still in the turn-on state, and D_{3b} and D_{4b} start conducting. In second stage the voltage across inductors is same.

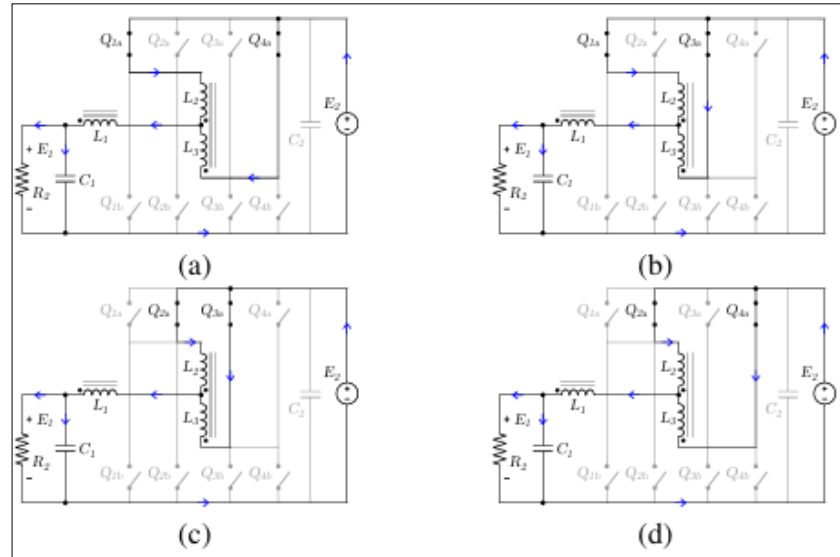


Fig 7: The suggested converter's topological stages for buck mode ($1/4 \leq D \leq 1/2$): a) state $[t_0, t_1]$ the states at times t_2, t_3, t_4, t_5 , and t_6 , and t_7

Stage Seven $[(t_6, t_7)]$; see Figure 7(d): At time t_6 , Q_{4a} is switched on, while Q_{2a} is still in the turn-on condition. The first stage is quite similar to this intermission. This pause is analogous to the initial, intermediate, and final phases.

Stage eight, as shown in Figure 6(e), is comparable to stage seven for the $D < 1/4$ area. At t_7 , D_{1b} and D_{2b} begin conducting, while Q_{4a} is still in the turn-on state, albeit Q_{2a} is switched off. As in the fourth step, the voltage across the inductors is the same.

To get the voltage gain, we use a volt-second balance on the magnetising inductor (8) and either (12) and (13) or (14) and

(12). Then, while the converter is operating in buck mode, the voltage gain is given by

$$M_2 = \frac{E_1}{E_2} = 2D \quad (15)$$

Comparing the DC voltage gain of the proposed converter in the buck working region to that of the traditional Buck converter which is identical to ^[18] as seen in Figure 8(b).

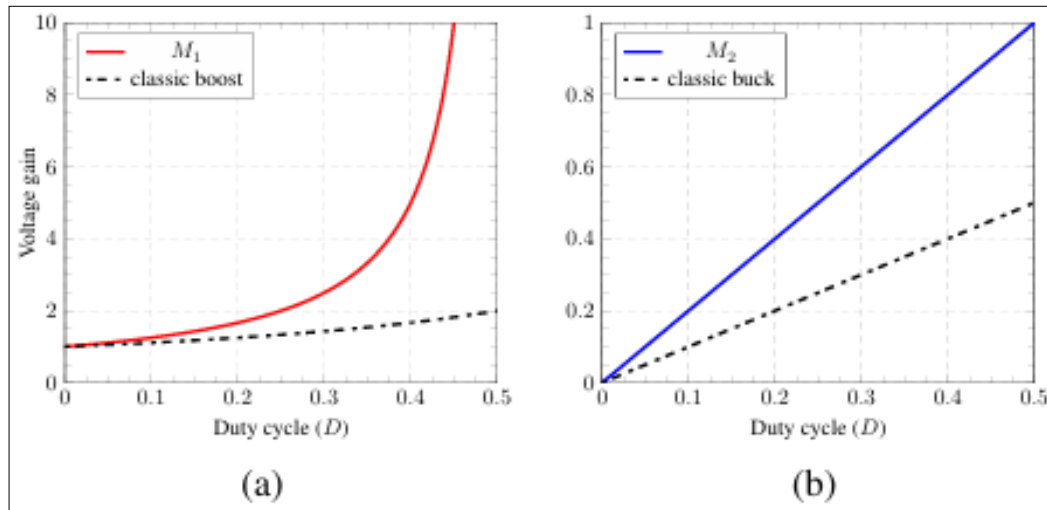


Fig 8: (a) Boost mode, (b) buck mode: DC voltage gain characteristics of the converter.

If the duty cycle is varied within the range of $1/4 \leq D < 1/2$, the input inductance (L_1) or current ripple (ΔI_{L1}) may be determined in boost mode for the CCM using equation (16).

$$L_1 = \frac{E_1 (4D - 1)}{4 \Delta I_{L1} f_s} \quad (16)$$

Simulation Results

The operational principles and the steady-state analysis are verified using OrCAD simulation. The simulation parameters for the operation in both directions are given in Table I. The simulation waveforms are shown as follow.

Table 1: Simulation parameters

S. No.	Parameter	Symbol	Value
1	Nominal Power	P	50 kW
2	Nominal Input Voltage	E1	200 V
3	Nominal Output Voltage	E2	600 V
4	Switching Frequency	f_s	20 kHz
5	Duty Cycle – Buck Mode	Dbuck	0.333
6	Duty Cycle – Boost Mode	Dboost	0.167
7	Input Voltage Ripple	ΔE_1	10 V
8	Output Voltage Ripple	ΔE_2	30 V
9	Inductor Current Ripple	ΔI_{L1}	30 A
10	Inductance	L_1	28 μ H
11	Inductance	L_2	26.5 μ H
12	Input Capacitance	C_1	5 μ F
13	Output Capacitance	C_2	12 μ F

As shown in Figure 9, the inductors' current waveforms during boost mode operation are displayed.

In Figure 10. Current via the load and voltage at the output.

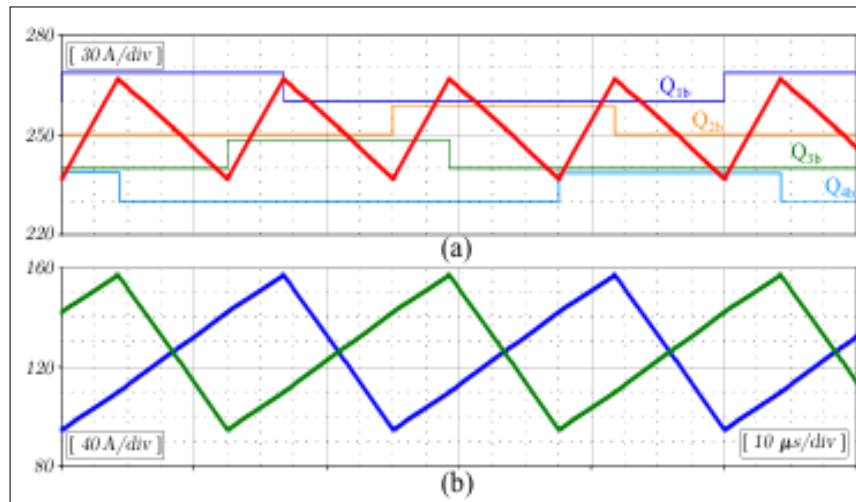


Fig 9: In boost mode operation, (a) the inductor current I_{L1} and the driving signals for the switches, and (b) the coupled inductor currents I_{L2} and I_{L3}

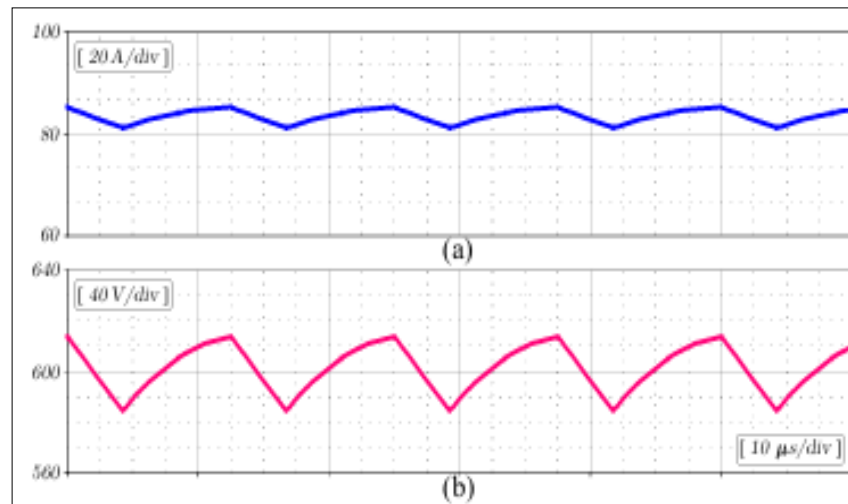


Fig 10: Functioning in boost mode: (a) output current I_{R1} , (b) output voltage E_2

With a duty cycle of 1/4 and the inductors operating in buck mode, the current waveforms are shown in Figure 11. At a duty cycle of 0.167 in buck mode, the ripple output voltage and current flowing from source E_2 are shown in Figure 12. Using the parameters from Table I, Table II compares the suggested architecture to existing circuits ^[19] operating in

boost mode. Minimal inductance, decreased dc-link capacitance, and low rms current on the devices are all features of the suggested. The interleaved converters' major drawbacks are the gate driver circuits and the abundance of semiconductor devices.

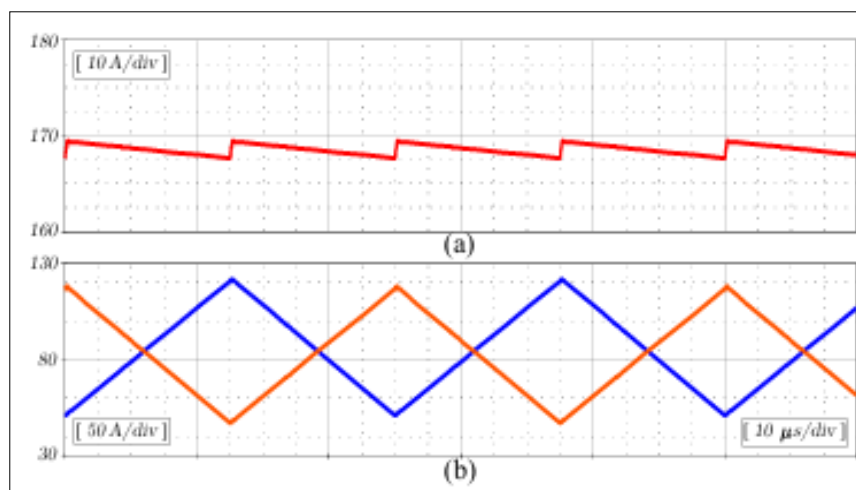


Fig 11: Operating in buck mode at $D=0.25$: (a) current via the output inductor I_{L1} (b) current thru the linked inductors I_{L2} and I_{L3}

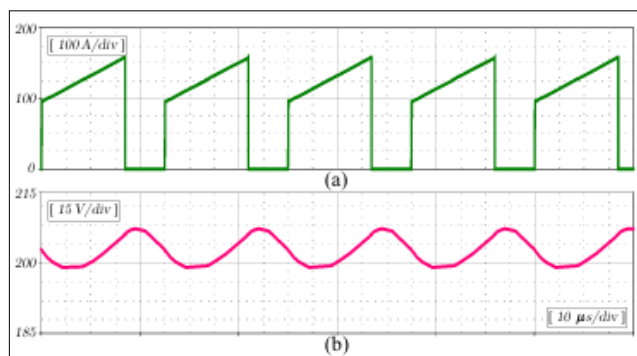


Fig 12: Operations in buck mode: (a) input current IE2 and (b) output voltage E1

Table 2: Comparison of the dc/dc converter topologies

Converter Topology	FS	Inductor L1	Current Ripple Frequency	Capacitor C2	Duty Cycle D	Switch/Diode Current
Classic Boost	80 kHz	55.5 μ H	fs	23.5 μ F	0.665	145 A
NCI	40 kHz	28.5 μ H	fs	12 μ F	0.664	104 A / 73 A
MDIBC	20 kHz	56 μ H	2fs	12 μ F	0.332	73.4 A / 36.7 A
Proposed Multiphase Converter	20 kHz	28 μ H	4fs	12 μ F	0.333	73.5 A / 36.7 A

The results show that the suggested multiphase converter uses only 28 μ H of input inductance while achieving the greatest effective current-ripple frequency of 4fs. As an added bonus, compared to the traditional boost converter, the semi-conductors experience much less current stress. These characteristics make the suggested architecture well-suited for high-power applications and point to an improvement in the utilisation of passive components.

Limitations

Control and implementation become more complicated due to the huge number of semiconductor switches and accompanying gate-driver circuits needed by the proposed multiphase bidirectional converter. In addition, the hypothesis of ideal components and continuous conduction mode (CCM) forms the basis of the theoretical analysis. Validation based on simulations is the major focus of this study. Various real-world considerations need experimental investigation, including switching losses, heat concerns, electromagnetic interference, and imperfect components.

Future Scope

The development and experimental validation of a hardware prototype under various operating and load situations will be the focus of future study. Advanced closed-loop control systems, phase-shedding techniques, and high-efficiency SiC/GaN semiconductor devices may be used to investigate further improvements in converter efficiency and power density. Electric cars, DC microgrids, renewable energy systems, and hybrid energy storage systems might all benefit from more testing of the suggested converter.

Conclusion

The study introduces a bidirectional dc/dc converter with multiphase interleaving and describes its operating concept for energy storage system applications. The converter allows for the energy storage devices and the external electrical system to transmit power in both directions. Thru ripple cancellation, the interleaving approach decreases conduction losses and the size of the capacitor/inductor. The simulation results verified that the suggested architecture can regulate the two-way power flow from the dc bus to the batteries/supercapacitors. These are

The simulation results show that the suggested converter can operate in both directions reliably. Boost mode involves shifting the input-current ripple to a higher effective frequency and achieving effective current sharing with the interleaved phase currents. The output voltage stays near to the necessary 600 V level, unaffected by switching ripple. In buck mode, the converter is able to smoothly move current from a high-voltage source to a low-voltage one while keeping the inductor current running continuously. The findings demonstrate the topology's appropriateness for high power bidirectional energy conversion and confirm the predicted operating principles.

some of the benefits that the newly developed converter circuit offers over its predecessors. (i) This design allows for two magnetic components and eight switches using antiparallel diodes to accomplish bidirectional power flow. (ii) Ripples in voltage and current are cut in half. (iii) Power electronic device current ratings are being reduced. (iv) There is room for improvement in the light load efficiency. It is possible to use the phase shedding method. The authors think the converter is competitive and suitable for niche uses like uninterruptible power supplies (UPSs) that need a lower input ripple current to keep their size, weight, and lifespan down, as well as high power (used above kW level) in electric, hybrid, or fuel cell vehicles.

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